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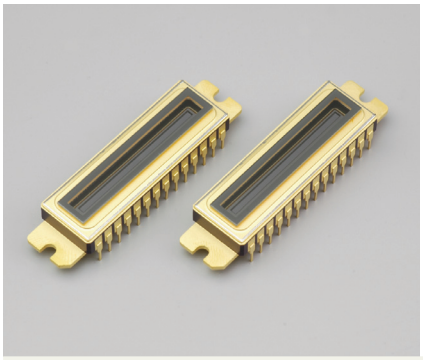
CCD image sensors



S11850-1106 S11851-1106

Improved etaloning characteristics, Constant element temperature control

The S11850/11851-1106 are back-thinned CCD image sensors designed for spectrometers. Two types consisting of a low noise type (S11850-1106) and high-speed type (S11851-1106) are available with improved etaloning characteristics. The S11850/11851-1106 offer nearly flat spectral response characteristics with high quantum efficiency from the UV to near infrared region. A thermoelectric cooler is placed inside the package to keep the element temperature constant (approx. 5 °C) during operation.

Features

- **Improved etaloning characteristics**
- **One-stage TE-cooled type (element temperature: approx. 5 °C)**
- **High sensitivity over a wide spectral range and nearly flat spectral response characteristics**
- **High CCD node sensitivity: 6.5 μV/e⁻ (S11850-1106) 8 μV/e⁻ (S11851-1106)**
- **High full well capacity, wide dynamic range (with anti-blooming function)**
- **Pixel size: 14 × 14 μm**

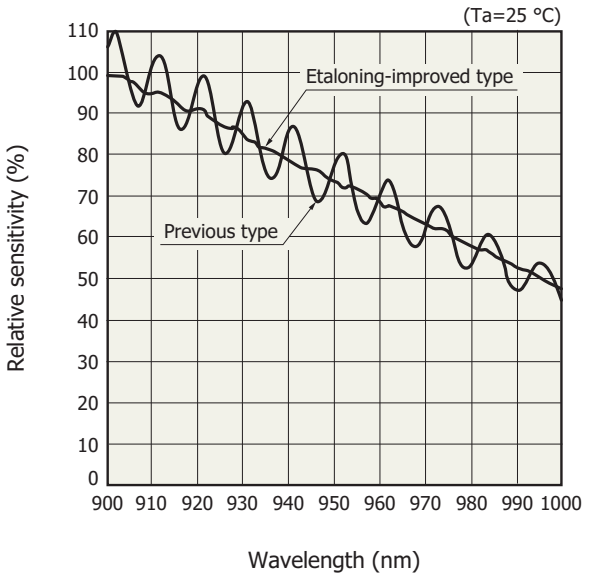
Applications

- **Spectrometers, etc.**

Improved etaloning characteristics

Etaloning is an interference phenomenon that occurs when the light incident on a CCD repeatedly reflects between the front and back surfaces of the CCD while being attenuated, and causes alternately high and low sensitivity. When long-wavelength light enters a back-thinned CCD, etaloning occurs due to the relationship between the silicon substrate thickness and the absorption length. The back-thinned CCDs (S11850/S11851-1106) have achieved a significant improvement in etaloning by using a unique structure that is unlikely to cause interference.

Etaloning characteristics (typical example)



Selection guide

Type no.	Total number of pixels	Number of effective pixels	Image size [mm (H) × mm (V)]	Readout speed max. (MHz)	Suitable driver circuit
S11850-1106	2068 × 70	2048 × 64	28.672 × 0.896	0.5	C11860
S11851-1106				10	-

Structure

Parameter	S11850-1106	S11851-1106
Image size (H × V)	28.672 × 0.896 mm	
Pixel size (H × V)	14 × 14 µm	
Number of total pixels	2068 × 70	
Numbe of effective pixels	2048 × 64	
Vertical clock phase	2-phase	
Horizontal clock phase	4-phase	
Output circuit	One-stage MOSFET source follower	Two-stage MOSFET source follower
Package	28-pin ceramic DIP (refer to dimensional outline)	
Window	Quartz glass*1	

*1: Hermetic sealing

Absolute maximum ratings (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage	S11850-1106	V_{OD}	-0.5	-	+30	V
	S11851-1106		-0.5	-	+25	
Reset drain voltage		V_{RD}	-0.5	-	+18	V
Output amplifier return voltage		Vret	-0.5	-	+18	V
Overflow drain voltage		V_{OFD}	-0.5	-	+18	V
Vertical input source voltage		V_{ISV}	-0.5	-	+18	V
Horizontal input source voltage		V_{ISH}	-0.5	-	+18	V
Overflow gate voltage		V_{OFG}	-10	-	+15	V
Vertical input gate voltage		V_{IG1V}, V_{IG2V}	-10	-	+15	V
Horizontal input gate voltage		V_{IG1H}, V_{IG2H}	-10	-	+15	V
Summing gate voltage		V_{SG}	-10	-	+15	V
Output gate voltage		V_{OG}	-10	-	+15	V
Reset gate voltage		V_{RG}	-10	-	+15	V
Transfer gate voltage		V_{TG}	-10	-	+15	V
Vertical shift register clock voltage		V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal shift register clock voltage		V_{P1H}, V_{P2H} V_{P3H}, V_{P4H}	-10	-	+15	V

*2: Chip temperature

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	S11850-1106			S11851-1106			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage			V_{OD}	23	24	25	12	15	18	V
Reset drain voltage			V_{RD}	11	12	13	14	15	16	V
Output amplifier return voltage*3			Vret				-	1	2	V
Overflow drain voltage			V_{OFD}	11	12	13	11	12	13	V
Test point	Input source		V_{ISV}, V_{ISH}	-	V_{RD}	-	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	-9	-8	-	V
Overflow gate voltage			V_{OFG}	0	12	13	0	13	14	V
Summing gate voltage		High	V_{SGH}	4	6	8	4	6	8	V
		Low	V_{SGL}	-6	-5	-4	-6	-5	-4	
Output gate voltage			V_{OG}	4	5	6	4	5	6	V
Reset gate voltage		High	V_{RGH}	4	6	8	4	6	8	V
		Low	V_{RGL}	-6	-5	-4	-6	-5	-4	
Transfer gate voltage		High	V_{TGH}	4	6	8	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	-9	-8	-7	
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	4	6	8	4	6	8	V
		Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH} V_{P3HH}, V_{P4HH}	4	6	8	4	6	8	V
		Low	V_{P1HL}, V_{P2HL} V_{P3HL}, V_{P4HL}	-6	-5	-4	-6	-5	-4	
Substrate voltage			V_{SS}	-	0	-	-	0	-	V
External load resistance			R_L	90	100	110	2.0	2.2	2.4	kΩ

*3: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	S11850-1106			S11851-1106			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Signal output frequency*4	fc	-	0.25	0.5	-	5	10	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	1200	-	-	1200	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H} C_{P3H}, C_{P4H}	-	160	-	-	160	-	pF
Summing gate capacitance	C_{SG}	-	10	-	-	10	-	pF
Reset gate capacitance	C_{RG}	-	10	-	-	10	-	pF
Transfer gate capacitance	C_{TG}	-	60	-	-	60	-	pF
Charge transfer efficiency*5	CTE	0.99995	0.99999	-	0.99995	0.99999	-	-
DC output level*4	Vout	17	18	19	7	8	9	V
Output impedance*4	Zo	-	10	-	-	0.3	-	kΩ
Power consumption*4 *6	P	-	4	-	-	75	-	mW

*4: The values depend on the load resistance. (S11850-1106: V_{OD}=24 V, R_L=100 kΩ, S11851-1106: V_{OD}=15 V, R_L=2.2 kΩ)
*5: Charge transfer efficiency per pixel, measured at half of the full well capacity
*6: Power consumption of the on-chip amplifier plus load resistance

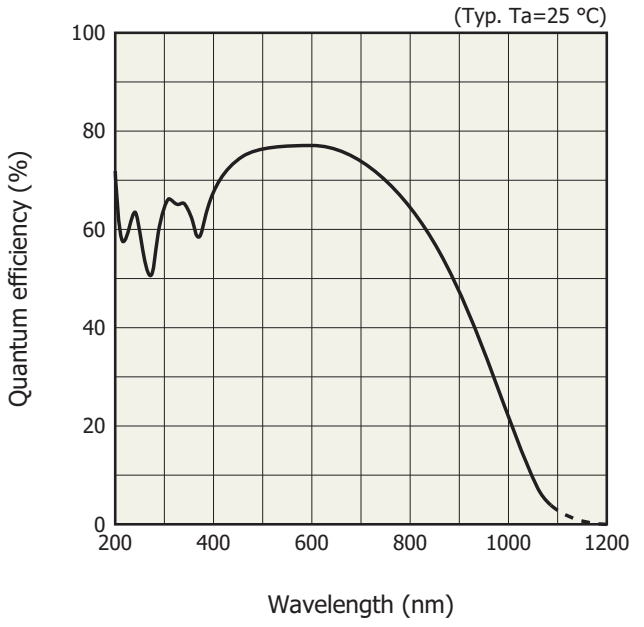
Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	S11850-1106			S11851-1106			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage		Vsat	-	Fw × CE	-	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	50	60	-	50	60	-	ke⁻
	Horizontal		250	300	-	150	200	-	
Conversion efficiency*7		CE	5.5	6.5	7.5	7	8	9	μV/e⁻
Dark current*8		DS	-	50	500	-	50	500	e⁻/pixel/s
Readout noise*9		Nread	-	6	15	-	23	28	e⁻ rms
Dynamic range*10	Line binning	Drange	41700	50000	-	6520	8700	-	-
Spectral response range		λ	-	200 to 1100	-	-	200 to 1100	-	nm
Photoresponse nonuniformity*11		PRNU	-	±3	±10	-	±3	±10	%

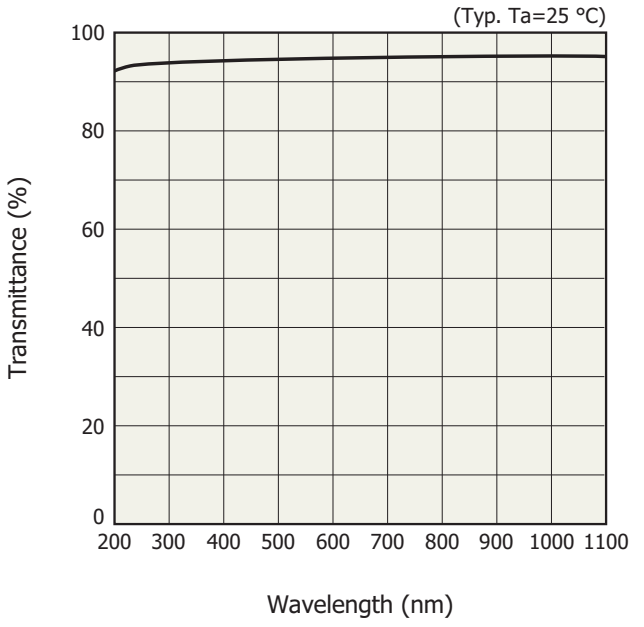
*7: The values depend on the load resistance. (S11850-1106: V_{OD}=24 V, R_L=100 kΩ, S11851-1106: V_{OD}=15 V, R_L=2.2 kΩ)
*8: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.
*9: S11850-1106: Td=-40 °C, fc=20 kHz, S11851-1106: Td=25 °C, fc=2 MHz
*10: Dynamic range = Full well capacity / Readout noise
*11: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

Spectral response (without window)*12

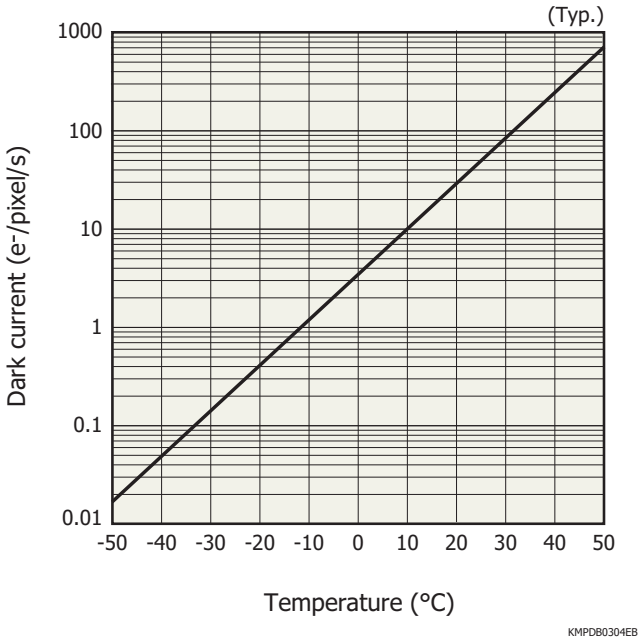


Spectral transmittance characteristics of window material



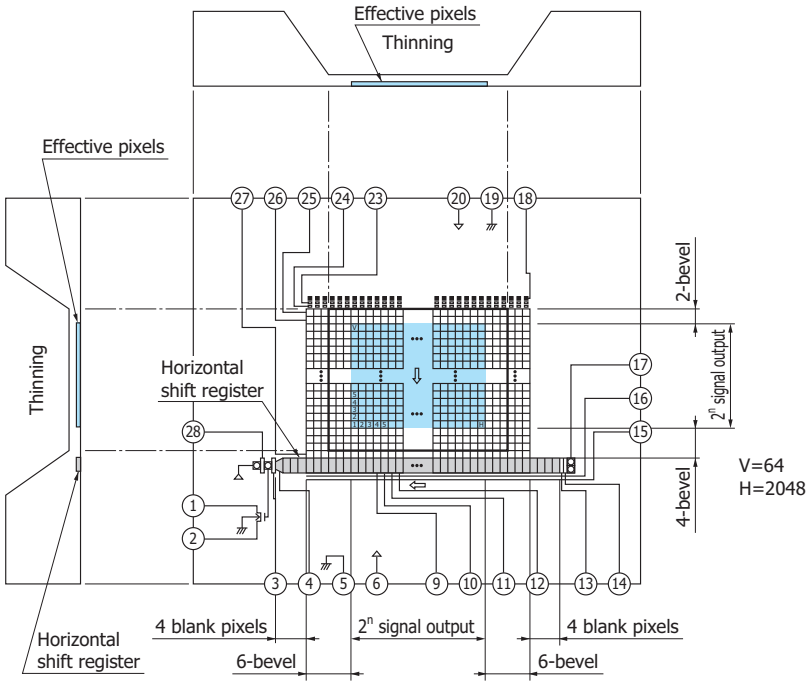
*12: Spectral response with quartz glass is decreased according to the spectral transmittance characteristics of window material.

Dark current vs. temperature



Device structure (conceptual drawing of top view in dimensional outline)

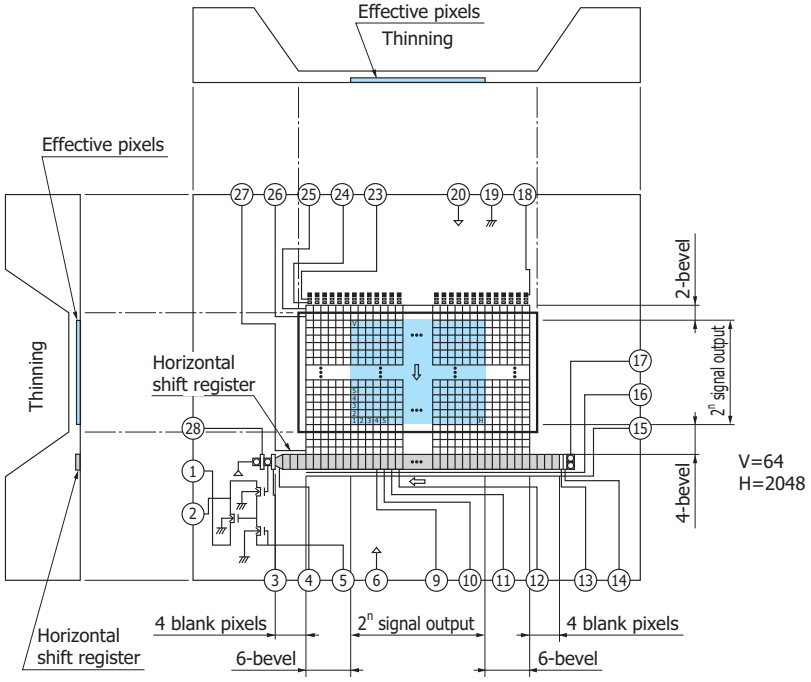
S11850-1106



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPDC0402EC

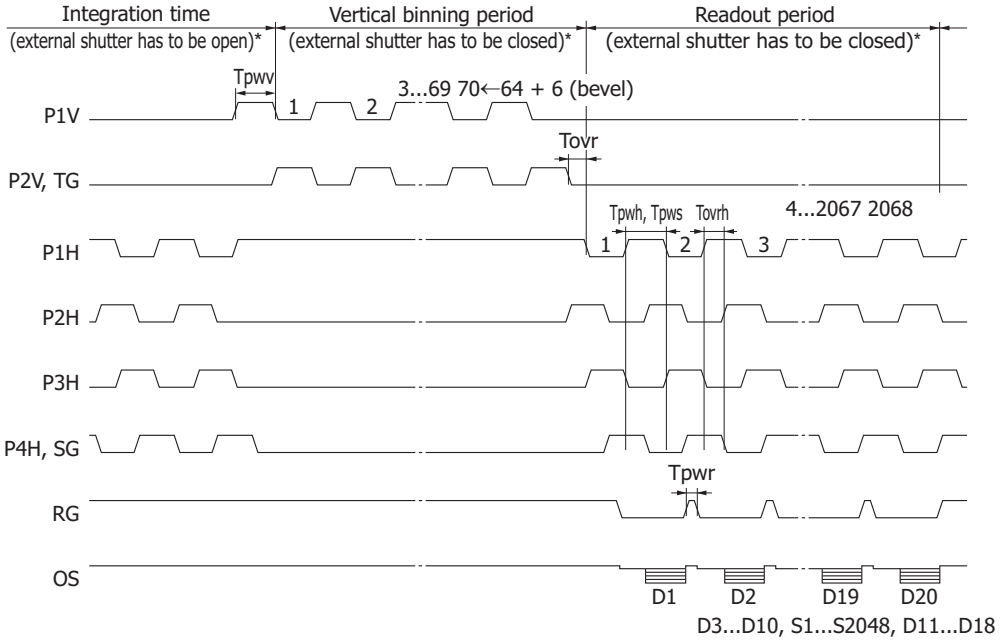
S11851-1106



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPDC0403EC

Timing chart (line binning)



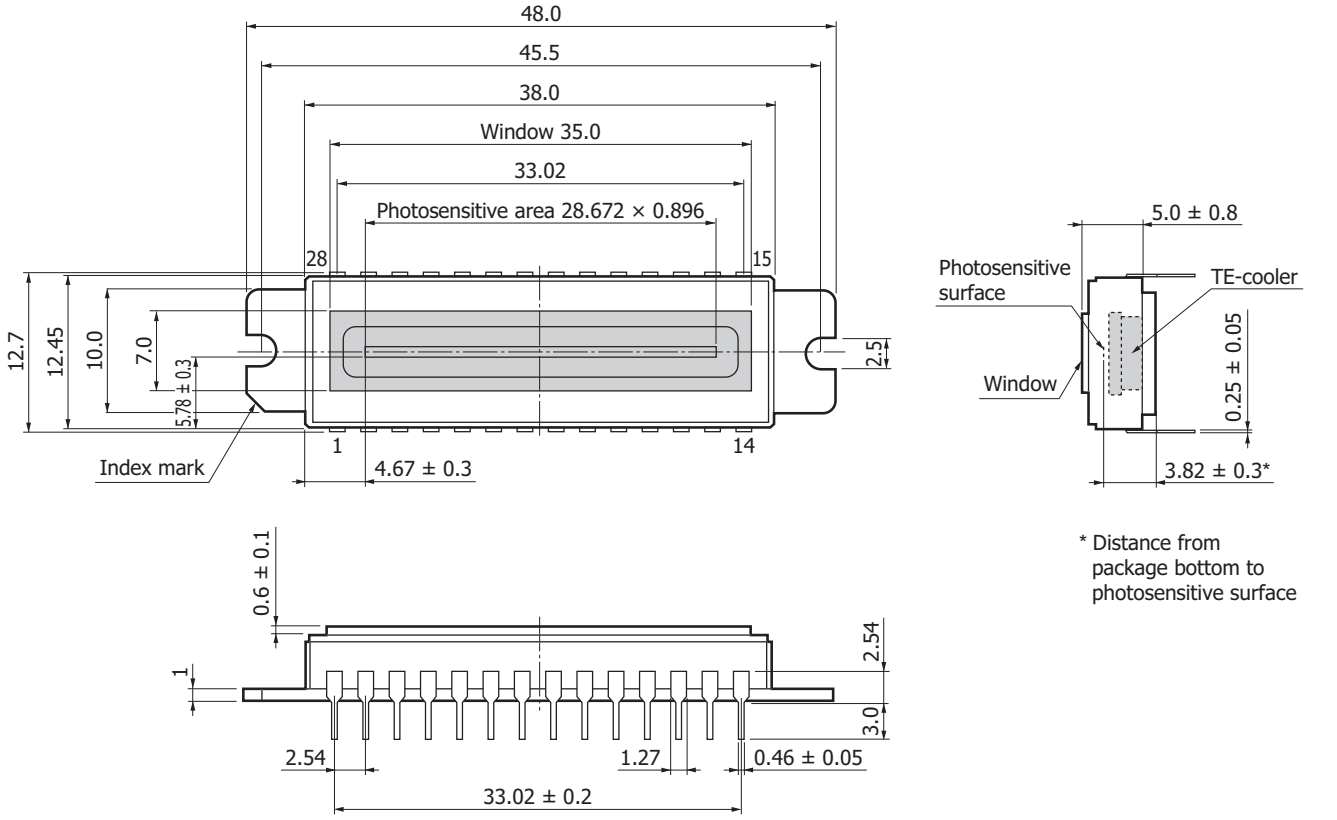
* An external shutter is not necessarily required.
When not using an external shutter, light entering during the vertical binning period and readout period is read out as signal.

KMPDC0404EA

Parameter		Symbol	S11850-1106			S11851-1106			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
P1V, P2V, TG	Pulse width*13	Tpwv	6	8	-	1	8	-	µs
	Rise and fall times*13	Tprv, Tpfv	20	-	-	20	-	-	ns
P1H, P2H, P3H, P4H	Pulse width*13	Tpwh	1000	2000	-	50	100	-	ns
	Rise and fall times*13	Tprh, Tpfh	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	25	50	-	ns
	Duty ratio*13	-	40	50	60	40	50	60	%
SG	Pulse width*13	Tpws	1000	2000	-	50	100	-	ns
	Rise and fall times*13	Tprs, Tpfs	10	-	-	10	-	-	ns
	Pulse overlap time	Tovrh	500	1000	-	25	50	-	ns
	Duty ratio*13	-	40	50	60	40	50	60	%
RG	Pulse width	Tpwr	100	1000	-	5	50	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	5	-	-	ns
TG-P1H	Overlap time	Tovr	1	2	-	1	2	-	µs

*13: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm, tolerance unless otherwise noted: ±0.15)



Pin connections

S11850-1106

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=100 kΩ
2	OD	Output transistor drain	+24 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	SS	Substrate	GND
6	RD	Reset drain	+12 V
7	Th1	Thermistor	
8	P-	TE-cooler-	
9	P4H	CCD horizontal register clock-4	
10	P3H	CCD horizontal register clock-3	
11	P2H	CCD horizontal register clock-2	
12	P1H	CCD horizontal register clock-1	
13	IG2H	Test point (horizontal input gate-2)	-8 V
14	IG1H	Test point (horizontal input gate-1)	-8 V
15	OFG	Overflow gate	+12 V
16	OFD	Overflow drain	+12 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	ISV	Test point (vertical input source)	Connect to RD
19	SS	Substrate	GND
20	RD	Reset drain	+12 V
21	P+	TE-cooler+	
22	Th2	Thermistor	
23	IG2V	Test point (vertical input gate-2)	-8 V
24	IG1V	Test point (vertical input gate-1)	-8 V
25	P2V	CCD vertical register clock-2	
26	P1V	CCD vertical register clock-1	
27	TG	Transfer gate	Same pulse as P2V
28	RG	Reset gate	

S11851-1106

Pin no.	Symbol	Function	Remark (standard operation)
1	OS	Output transistor source	RL=2.2 kΩ
2	OD	Output transistor drain	+15 V
3	OG	Output gate	+5 V
4	SG	Summing gate	Same pulse as P4H
5	Vret	Output amplifier return	+1 V
6	RD	Reset drain	+15 V
7	Th1	Thermistor	
8	P-	TE-cooler-	
9	P4H	CCD horizontal register clock-4	
10	P3H	CCD horizontal register clock-3	
11	P2H	CCD horizontal register clock-2	
12	P1H	CCD horizontal register clock-1	
13	IG2H	Test point (horizontal input gate-2)	-8 V
14	IG1H	Test point (horizontal input gate-1)	-8 V
15	OFG	Overflow gate	+13 V
16	OFD	Overflow drain	+12 V
17	ISH	Test point (horizontal input source)	Connect to RD
18	ISV	Test point (vertical input source)	Connect to RD
19	SS	Substrate	GND
20	RD	Reset drain	+15 V
21	P+	TE-cooler+	
22	Th2	Thermistor	
23	IG2V	Test point (vertical input gate-2)	-8 V
24	IG1V	Test point (vertical input gate-1)	-8 V
25	P2V	CCD vertical register clock-2	
26	P1V	CCD vertical register clock-1	
27	TG	Transfer gate	Same pulse as P2V
28	RG	Reset gate	

Specifications of built-in TE-cooler (Typ., vacuum condition)

Parameter	Symbol	Condition	Specification	Unit
Internal resistance	Rint	Ta=25 °C	1.6	Ω
Maximum current*14 *15	Imax	Tc*16=Th*17=25 °C	1.8	A
Maximum voltage	Vmax	Tc*16=Th*17=25 °C	3.5	V
Maximum heat absorption*18	Qmax		4.0	W

*14: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.
*15: To ensure stable temperature control, ΔT (temperature difference between Th and Tc) should be less than 30 °C. If ΔT exceeds 30 °C, product characteristics may deteriorate. For example, the dark current uniformity may degrade.
*16: Temperature of the cooling side of thermoelectric cooler
*17: Temperature of the heat radiating side of thermoelectric cooler
*18: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

Specifications of built-in temperature sensor

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: Resistance at absolute temperature T1 [K]
R_{T2}: Resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.

R_{298}=10 kΩ
$B_{298/323}$=3900 K

Precautions

· If the thermoelectric cooler does not radiate away sufficient heat, then the product temperature will rise and cause physical damage or deterioration to the product. Make sure there is sufficient heat dissipation during cooling. As a heat dissipation measure, we recommend applying a high heat-conductivity material (silicone grease, etc.) over the entire area between the product and the heatsink (metallic block, etc.), and screwing and securing the product to a heatsink.
· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
· Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
· Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

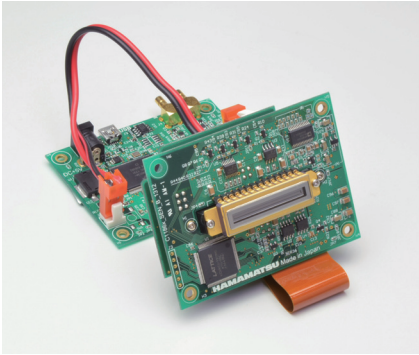
■ Precautions
· Disclaimer
· Image sensors

■ Technical information
· FFT-CCD area image sensor

Driver circuit C11860 (sold separately) for CCD image sensor (S11850-1106, S14651 series)

The C11860 is a driver circuit developed for the Hamamatsu CCD image sensor S14651 series and S11850-1106.

Features



- **Built-in 16-bit A/D converter**
- **The sensor circuit board and interface circuit board are connected using a flexible cable.**
- **Interface: USB 2.0**
- **External synchronization capable**
- **Single power supply: +5 VDC**
- **Sensor cooling control (approx. +5 °C)**

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